Online Exam Questions

8th BELAS Summer School, June 20-22, 2018

http://tallinn2018.belas-event.org/program/online-exam

You can answer one or several questions at a time and will be able to edit your answers anytime until the cut-off deadline - **June 25, 23:59** anywhere in the world. Please click the SUBMIT button at the last page for your answers to be saved, the system will provide you with a link to come back and edit/continue and will also send you a copy by email. A phrase or a short text of up to a couple of sentences is sufficient as an answer.

You are strongly encouraged to start answering already during the event!

After your final answers are evaluated by the lecturers, you will receive a notification email with your scores and will be able to get to the answers to see the detailed results.

Timeline:

June 20-25: Online-exam is open for answers
June 26 - July 3: Evaluation by the lecturers
July 5: Scores released to the participants

Questions

1-a (R. Velazco): Miniaturization is a deal to state of the art design or architectural radiation hardening techniques?

1-b (R. Velazco): Should Internet of Things developers consider the errors provoked by neutrons present in our atmosphere as potential sources of critical errors?

2-a (P. Rech): Explain the concept of critical and non-critical Silent Data Corruption and give examples of application that could intrinsically tolerate some type of errors.

2-b (P. Rech): Are novel parallel computing architecture more or less complex to be tested than traditional CPU/micro-controllers? Why?

2-c (P. Rech): Are transient faults better or worse than permanent faults? Explain your answer.

3-a (F. Vargas): In your opinion, why is it important to perform combined tests for ionizing and non-ionizing radiation if one is designing an embedded system for aerospace applications?

3-b (F. Vargas): Up to date there is no standard that recommends combined tests for electronics devoted to critical applications, such as aerospace. So, how can you explain the fact that satellites and airplanes are still flying apparently without any problem or need of such combined tests?

3-c (F. Vargas): Consider two technologies: (a) CMOS 600nm and (b) CMOS 22nm and answer the following questions. Which of these technologies suffers more from SEU than TID? Why? Which of these technologies suffers more from TID than SEU? Why?

4-a (Z. Navabi): What are the most important distinguishing factors of a programming and a hardware description language? How is SystemC solving this problem?

4-b (Z. Navabi): What is a SystemC channel? How does a channel bind two SystemC modules?

4-c (Z. Navabi): How do interface methods of SystemC channels help deciding on Processing Element communications in Design Space Exploration?

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(Optional) **4-d (Z. Navabi):** Write SystemC description for an 8-bit adder with two *ain* and *bin* 8-bit operands, and 8-bit *sum*, and a 1-bit *carryout*.

5-a (M. Michael): Name 3 sources of reliability risks in current CMOS ICS and briefly explain how each one affects the operation of an IC.

5-b (M. Michael): Briefly describe the main categories of on-line fault detection methods in modern microprocessor systems. What at the main advantages and disadvantages of each category?

5-c (M. Michael): What is self-test and what are its main uses? What is software-based self-test (SBST)? What is selective SBST and what are its advantages/disadvantages wrt standard SBST?

6-a (A. Jutman): What is an embedded instrument? Give some examples. Put them in context of system health monitoring.

6-b (A. Jutman): Does a fault tolerant system have to support graceful degradation and be self-health aware? Why?

7-a (M. Glorieux): How the criticality of a ISO26262 compliant system is evaluated? What are the expected functional failure rates for each class of criticality?

7-b (M. Glorieux): Let's assume that any functional failure leads to 50 seconds of outage. What is the FIT target corresponding to a "six nines" availability? (detail the calculations)

7-c (M. Glorieux): Let's consider a SRAM of 65536 words of 36 bits, implemented with a multiplexing factor of 2, protected by SECDED ECC; and the following per cell error rates:

- SBU: 300 FIT/Mbit
- MBU2: 15 FIT/Mbit
- MBU3: 4 FIT/Mbit
- MBU4: 1 FIT/Mbit
- MBU5: 0.3 FIT/Mbit

What are corrected, detected and not detected error rates for the whole SRAM? (detail the calculations)

8-a (A. Klotz): What are the key support instruments for commercial EDA tools (on example of Cadence tools) different from academic open-source initiatives?

8-b (A. Klotz): What is the advantages of using Process Development Kit (PDK) in IC design flow?

8-c (A. Klotz): What is the impact of OpenAccess API on IC design flows?

9-a (V. Champac): What are two important performance characteristics offered by FinFET technology?

9-b (V. Champac): Mention two type of manufacturing defects relevant for FinFET.

10-a (M. Kruusmaa): What is the difference between paraphrasing, summarizing and quoting?

10-b (M. Kruusmaa): Please describe at least three research activities which constitute an significant intellectual contribution to a paper (and therefore warrant an authorship).

10-c (M. Kruusmaa): What are the responsibilities of a (co)author of a scientific publication?

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